Polyhedral compilation to systolic arrays

PolySA and AutoSA

Basic Idea

PolySA and AutoSA are two papers that auto-generate systolic arrays for implementation on FPGAs, from a polyhedral model input

(They are by the same people)

The polyhedral model can be used for transforming nested loops so as to extract parallelism

PolySA and AutoSA take this a step further and extract parallelism explicitly with the purpose of mapping it to systolic arrays

One view of the polyhedral model

Take a polyhedron of points, with some affine dependencies and so forth, and:

Find tiling "hyperplanes" which have an execution order that respects dependencies

Or, equivalently, find an affine transformation such that in the new space, rectangular blocking is such a tiling

Optimize such that distance (in blocks) of dependencies is minimized

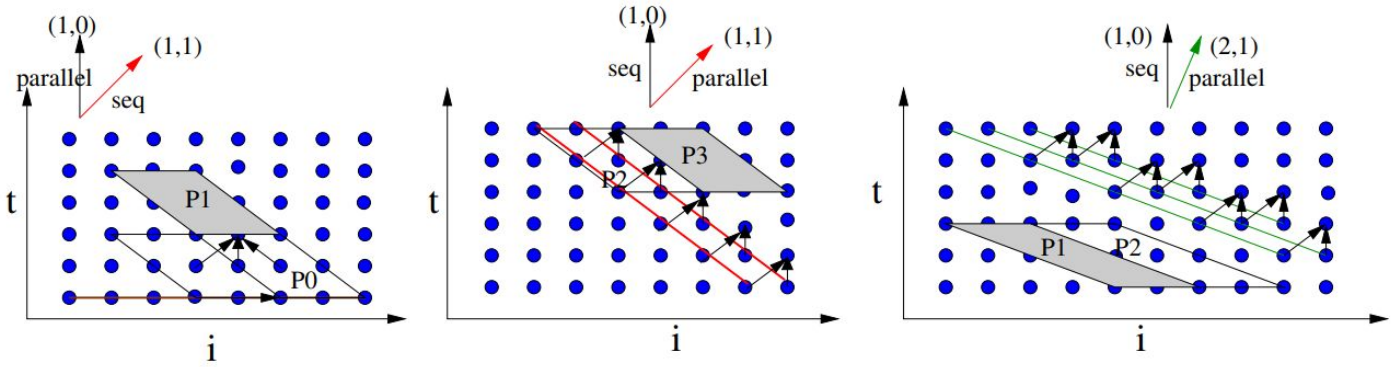

Figure 3. Communication volume with different valid hyperplanes for 1-d jacobi